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10/593,577	09/20/2006	Kiyoshi Kato	0756-7839	1460

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,577	KATO, KIYOSHI	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-13 and 19-28* is/are rejected.

7)☒ Claim(s) *7 and 14-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL REJECTION

Claims Rejections

Claim Rejections - 35 USC § 112

Claims 7 and 14-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 7, it is not understood how the "connecting terminal" can control an amount of charge on line 2 since the connection terminal is only an "end" or an "input" which cannot perform the function of controlling charge. The same is true for claims 14-18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 and 8-9 are rejected under 35 USC 102 (e) as being anticipated by Hirata (US 6,670,679).

Regarding claims 1-2, 10 Hirata discloses in Figures 4 and 9-12A a circuit comprising:

- a transistor (104, 104a in Figure 10 or 60 in Figure 12A) having a floating gate (106, 106a in Figure 10 or 55 in Figure 12A) and a control gate (105, 105a in Figure 10 or 57 in Figure 12A), wherein the floating gate (55, Figure 12A) and the control gate (57) of the transistor (60)

overlap each other with an insulating film (56, Figure 12A) interposed therebetween; a drain or a source of the transistor is connected to the control gate; and the drain and the control gate are connected to an input terminal (32) and an output terminal, see Figure 10. Wherein the transistors (104, 104a) are thin film transistors.

- Regarding claim 8, wherein a resistor (107) is connected to the floating gate (106).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-13 and 19-28 are rejected under 35 USC 103 (a) as being unpatentable over Hirata (US 6,670,679) in view of Ueno et al (US 6,300,656).

Regarding claims 1-2 and 10, Hirata discloses in Figures 4 and 9-12A a circuit comprising:

- a transistor (104, 104a in Figure 10 or 60 in Figure 12A) having a floating gate (106, 106a in Figure 10 or 55 in Figure 12A) and a control gate (105, 105a in Figure 10 or 57 in Figure 12A), wherein the floating gate (55, Figure 12A) and the control gate (57) of the transistor (60) overlap each other with an insulating film (56, Figure 12A) interposed therebetween; a drain or a source of the transistor is connected to the control gate; and the drain and the control gate are

connected to an input terminal (32) and an output terminal, see Figure 10. Wherein the transistors (104, 104a) are thin film transistors.

However, Hirata does not disclose that a side surface of the floating gate is covered with a third insulation film , and a plurality of transistors are connected in series so as to have the same forward current direction. For example, Figure 10 of Hirata shows each transistor (104) includes only one transistor.

Nevertheless, Ueno et al suggests in Figure 1 a MOS transistor is formed with a floating gate (4), a control gate (6), insulating films (3, 5), and a third insulating film (7) covering sides surface of the floating gate (4), see lines 25-35, column 13, for reducing a longitudinal electric field at a point where a lateral electric field has a peak and the most hot electrons generate so as to increase a probability with which generated high energy electrons are injected into a floating gate electrode, see lines 58-65, column 4.

It would have been obvious to a person having skill in the art at the time the invention was made to form the MOS transistor of Hirata as suggested by Ueno et al for the purpose of reducing a longitudinal electric field at a point where a lateral electric field has a peak and the most hot electrons generate so as to increase a probability with which generated high energy electrons are injected into a floating gate electrode.

Since the transistor (104) Hirata is connected as a diode to provide a voltage drop of .3V-.7V volt on a shunt path when it is on, a skilled artisan realizes that cascaded transistors can be used to increase voltage drops to adjust the shunt current. Thus, employing a plurality of transistors in series as claimed is considered to be a matter of a design expedient for an engineer depending upon a particular application in which the circuit of Hirata is to be used. It would have

been obvious to a person having skill in the art at the time the invention was made to employ a plurality of transistors as claimed for the purpose of increasing voltage drops.

Regarding claims 3-6, wherein the plurality of transistors (104, 104a) of Hirata are connected in series as shown in Figure 10.

Regarding claims 8, 13 and 19-23, since the resistor is a means for reducing current, a skilled artisan would have recognized that a resistor can be placed between the input and the drain of the transistor of Hirata for providing an over-current protection for this transiston. Thus, placing a resistor between the input and the drain terminal of the transistor of Hirata as claimed is considered to be a matter of a design expedient that would have been obvious at the time of the invention.

Regarding claims 10-12, since the circuit of Hirata is a protective circuit; obviously it may be used in a communication circuit comprising an antenna for protecting the communication circuit. Thus, employing the circuit of Hirata for protecting a predetermined communication circuit comprising an antenna is considered to be a matter of a design expedient for an engineer that would have been obvious at the time of the invention.

Regarding claims 24-28, wherein the modified transistor of Hirata in view of Ueno et al is a thin film transistor.

Response to Applicant's

The applicant argues Hirata does not teach, either explicitly or inherently, or suggest all the features of the independent claims, as amended. Independent claims 1-6, 10 and 11 have been amended to recite that a floating gate is formed over a semiconductor layer with a first insulating

film interposed therebetween,the floating gate and a control gate overlap each other with a second insulating film interposed therebetween, a side surface of the floating gate is covered with a third insulating film, and the floating gate is insulated from the semiconductor layer. The arguments are not persuasive because these limitations are suggested by Ueno et al as stated above.

Allowable Subject Matter

Claims 7 and 14-18 would be allowable if rewritten or amended to overcome the rejection under 35 USC, 112 second paragraph, as set forth above and include all of the limitations of the base claim. This claim is allowed because the prior art of record fail to suggest a connecting terminal for controlling charge accumulated in the floating gate in combination as claimed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, can be reached at (571) 272-1736.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DINH T. LE/

Primary Examiner, Art Unit 2816